IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 10/212,903, filed August 5, 2002, ~~pending,~~ now U.S. Patent 6,611,467, issued August 26, 2003, which is a continuation of application Serial No. 09/977,755, filed October 15, 2001, now U.S. Patent 6,442,086, issued August ~~27,2002,~~ 27, 2002, which is a continuation of application Serial No. 09/897,360, filed July 2, 2001, now U.S. Patent ~~6,327,201 B2,~~ 6,327,201, issued December 4, 2001, which is a continuation of application Serial No. 09/583,478, filed May 31, 2000, now U.S. Patent 6,256,242, issued July 3, 2001, which is a continuation of application Serial No. 09/392,154, filed September 8, 1999, now U.S. Patent 6,101,139, issued August 8, 2000, which is continuation of application Serial No. 09/026,244, filed February 19, 1998, now U.S. Patent 6,002,622, issued December 14, 1999.

Please amend paragraph number **[0006]** as follows:

[0006] Once the memory cells attached to the complementary digit lines D0*, D1*, etc. have been tested, the memory cells attached to the true digit lines D0, D1, etc. are tested by firing the row line R1, for example. This causes the memory cells attached to the row line R1 to dump their stored charge from their memory cell capacitors 12 onto the complementary digit lines D0*, D1*, etc. In turn, this causes the sense amplifiers 14 to pull each of the complementary digit lines D0*, D1*, etc. up to the supply voltage V_{CC}, and to pull each of the true digit lines D0, D1, etc. down to ground. As a result, a full V_{CC}-to-ground voltage drop is imposed across NMOS access devices 18 of the memory cells attached to the true digit lines D0, D1, etc. The ~~V_{CC}-to-ground~~ V_{CC}-to-ground voltage drop is maintained across the NMOS access devices 18 for another predetermined refresh interval of about 150 to 200 ms. This stresses any "leaky" NMOS access devices 18 and causes any such NMOS access devices 18 to lose significant charge from their memory cell capacitors 12 to the true digit lines D0, D1, etc. to which they are attached.

Please amend paragraph number **[0008]** as follows:

[0008] This conventional margin testing method thus typically takes two predetermined refresh intervals of about 150 to 200 ms. each to complete. Since row lines in different ~~sub-arrays~~ sub-arrays in a semiconductor memory typically cannot be fired simultaneously because the addressing of the row lines is local to their respective sub-arrays, this conventional method cannot be used on more than one sub-array at a time. As a result, in a semiconductor memory containing four sub-arrays, for example, the conventional method described above takes approximately 1.2 to 1.6 seconds to complete. Because of the large number of semiconductor memories that typically require margin testing during production, it would be desirable to find a margin testing method that can be completed more quickly than the method described above.

Please amend paragraph number **[0017]** as follows:

[0017] In another embodiment of the ~~invention a~~ invention -- a method of margin testing a ~~DRAM a~~ DRAM -- a high voltage level is stored in memory cells of the DRAM. Equilibrating circuitry in sense amplifiers of the DRAM is isolated from an equilibrate bias node of the DRAM and from a cell plate voltage thereon, and a ground voltage from within the DRAM is applied to the equilibrating circuitry in each sense amplifier. Digit line pairs of the DRAM are then equilibrated to the ground voltage using the equilibrating circuitry in each sense amplifier, and the digit line pairs are held at the ground voltage for a predetermined refresh interval in order to stress the memory cells of the DRAM, which are attached to the digit line pairs. After the predetermined refresh interval has passed, all the memory cells of the DRAM are read to identify those that have failed the margin test. The refresh interval may be, for example, about 150 to 200 milliseconds.

Please amend paragraph number **[0018]** as follows:

[0018] In still another embodiment of the ~~invention a~~ invention -- a method of testing a semiconductor ~~memory a~~ memory -- a substantially identical logic voltage is stored in all memory cells of the semiconductor memory. Also, digit line pairs of the semiconductor memory

that are attached to the memory cells are isolated from a digit line equilibrating bias voltage. This is accomplished by deactivating an NMOS transistor coupled between the bias voltage and the digit line pairs, or by failing to activate equilibrate circuitry coupled between the bias voltage and the digit line pairs that normally is activated during memory operations of the semiconductor memory. A stressing voltage from within the semiconductor memory that is substantially different than the logic voltage stored in the memory cells is then applied to all the digit lines of all the digit line pairs at substantially the same time, thereby stressing the memory cells. The digit line pairs are held at the stressing voltage for a predetermined interval, and all the memory cells of the semiconductor memory are then read to identify those that have failed the test.